
THE COARSE-GRAINED / FINE-GRAINED LOGIC INTERFACE IN FPGAS WITH EMBEDDED FLOATING-POINT ARITHMETIC UNITS

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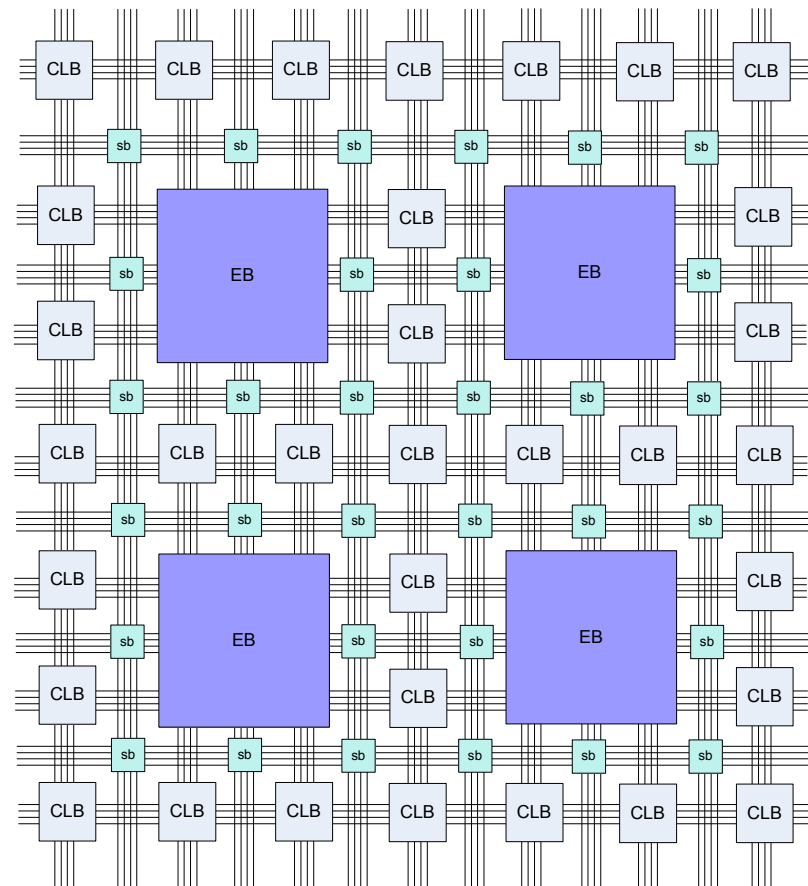
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Outline

1. Motivation
2. Background
3. Contributions
4. Architecture assumptions
5. Interface parameters
6. Exploration tool
7. Benchmarks
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9. Conclusion

1. Motivation

- Interface between coarse-grained and fine-grained is important to an FPGA
- Not flexible enough : reduce usefulness of coarse-grained block
- Too flexible : result in unnecessary overhead for applications that do not use the embedded component



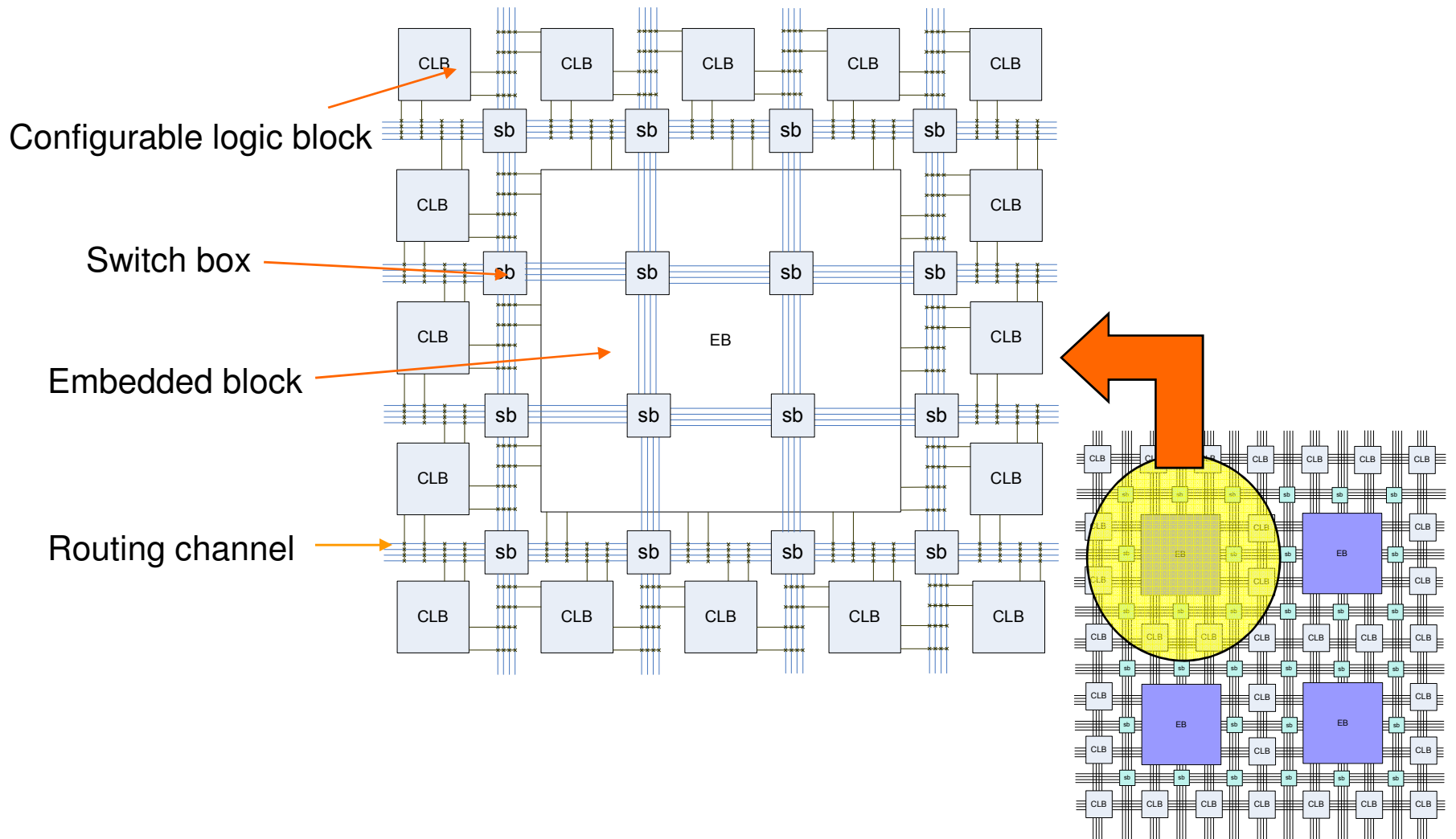
2. Background

- Adding coarse-grained block within the fine-grained fabric FPGA improves area and delay
- Novel domain-specific hybrid FPGA architecture that targets floating point applications improves 18 times area-efficient
- Few have examined the interface between the coarse-grained blocks and fine-grained fabric

3. Contributions

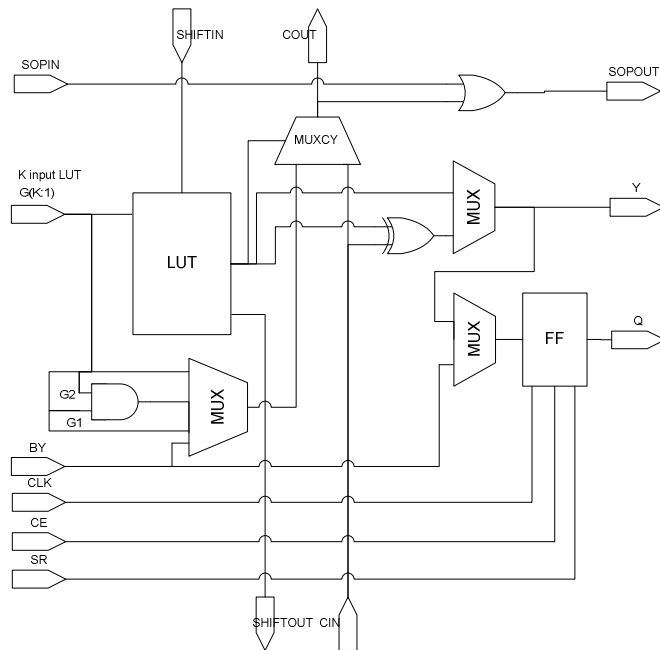
- A set of parameters that describes the interface between coarse-grained and fine-grained programmable logic in FPGAs
- An empirical framework to model the impact of coarse-grained architectural parameters in terms of performance, density, and power consumption
- An empirical study that examines the set of parameters

4. Architecture assumption -Hybrid FPGA

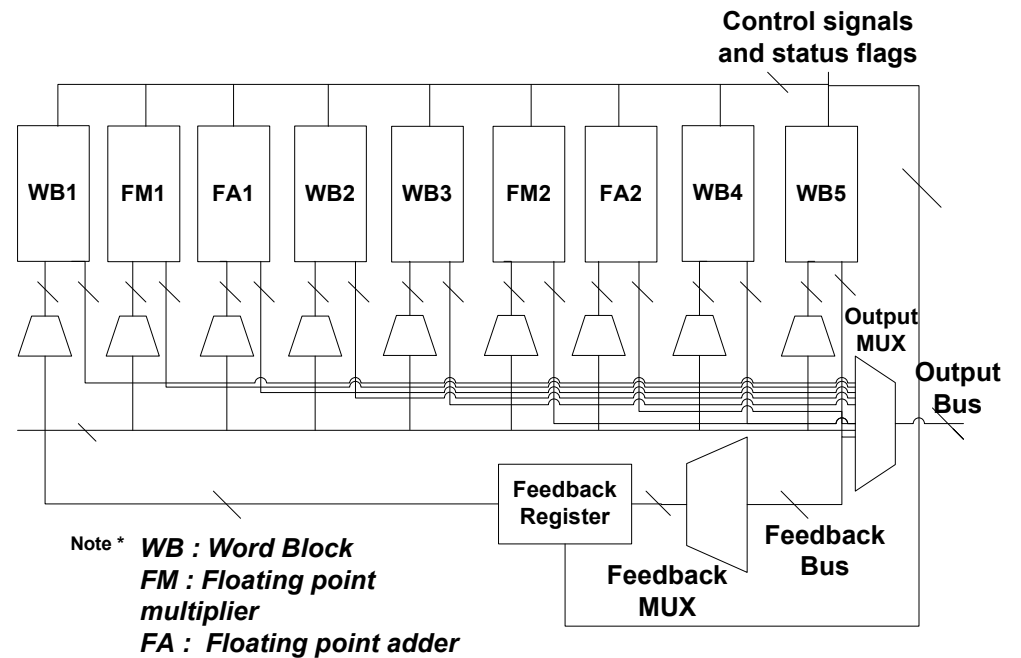


Architecture assumption – Coarse/Fine-Grained

- Fine-Grained (configurable logic block)

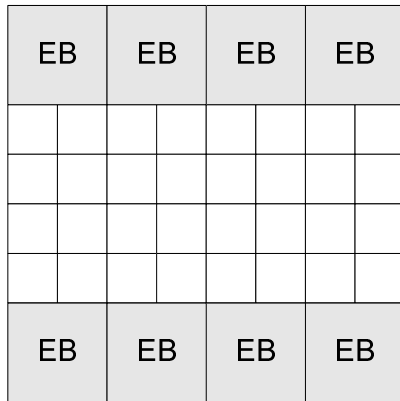


- Coarse-Grained (64 bits floating point block, 182 tiles, 9.2ns)

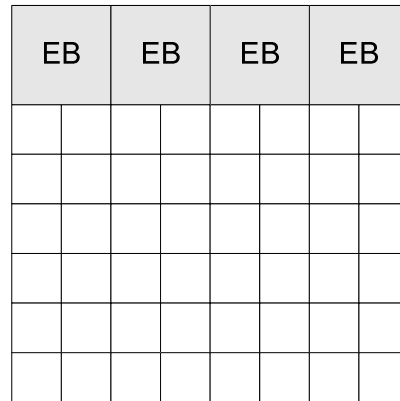


5. Interface parameters – 1

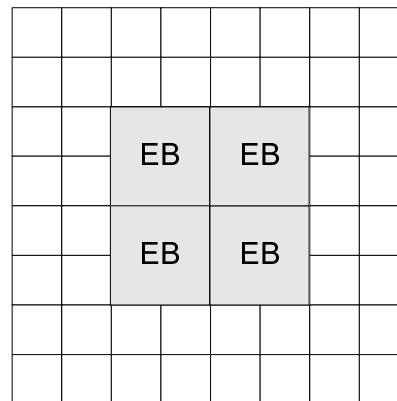
EB Position



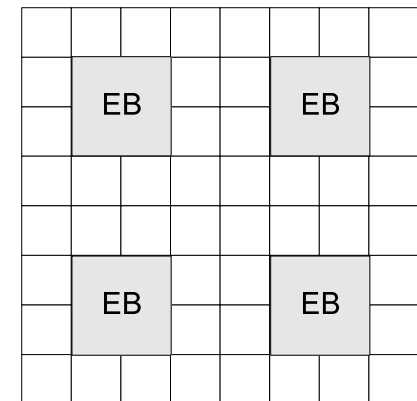
(a) Type 1: EBs are on the top and bottom of CLBs



(b) Type 2: All EBs are on the top of CLBs



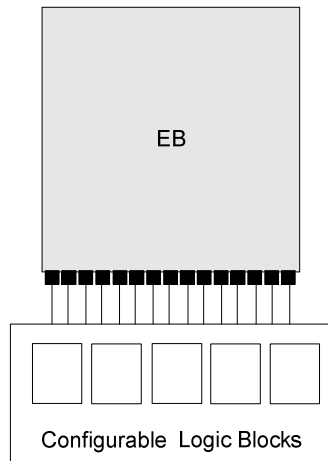
(c) Type 3: EBs are in the middle of CLBs



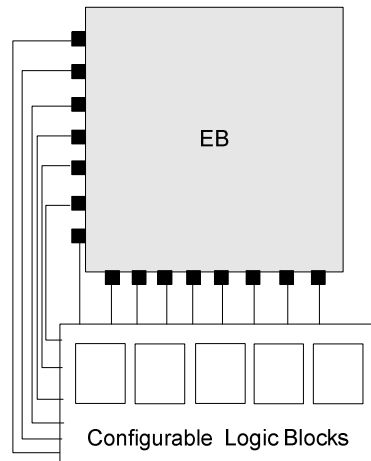
(d) Type 4: EBs are surrounded by sea of CLBs

Interface parameters – 2

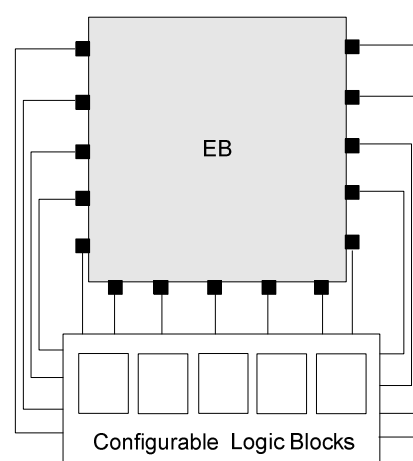
Pin Location



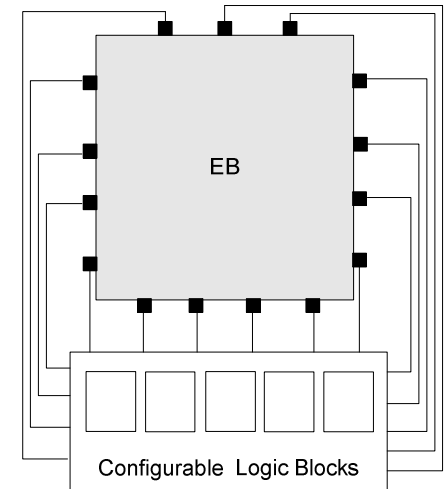
(a) CLBs connect to one side of EB with highest I/O density



(b) CLBs connect to two sides of EB



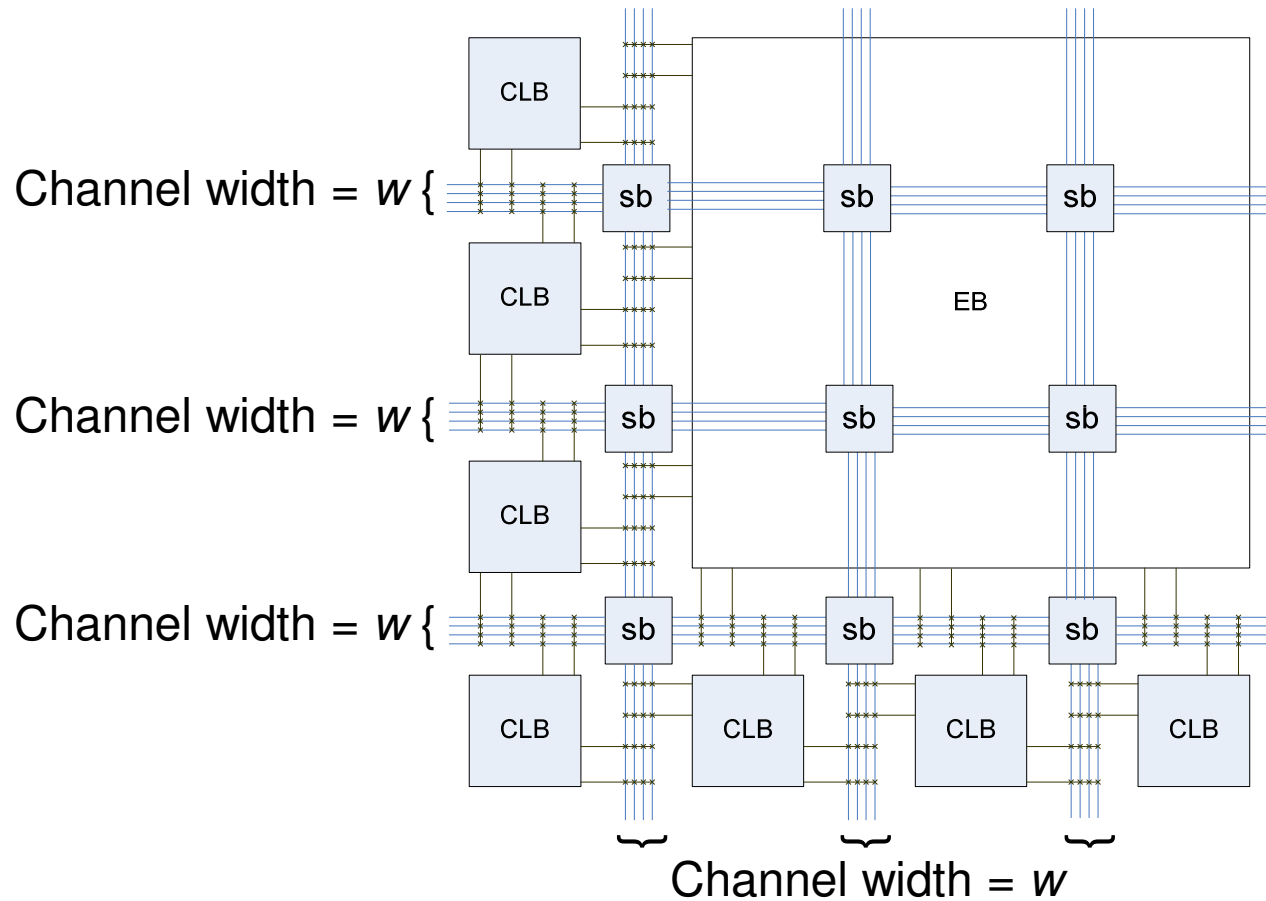
(c) CLBs connect to three sides of EB



(d) CLBs connect to four sides of EB with lowest I/O density

Interface parameters – 3

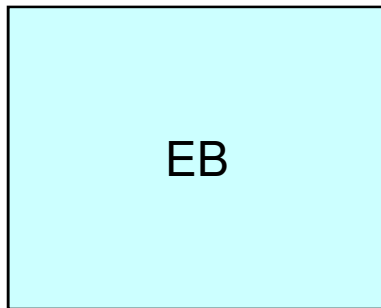
Interconnect Flexibility



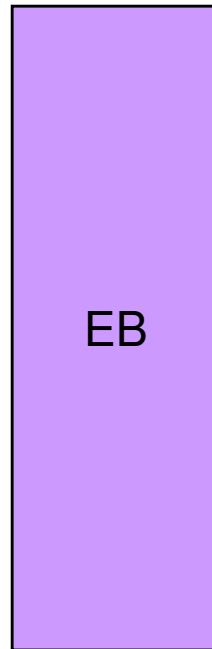
Interface parameters – 4

Shape

Area \approx 182 CLBs



(a) 13x14 CLBs



(b) 7x26 CLBs

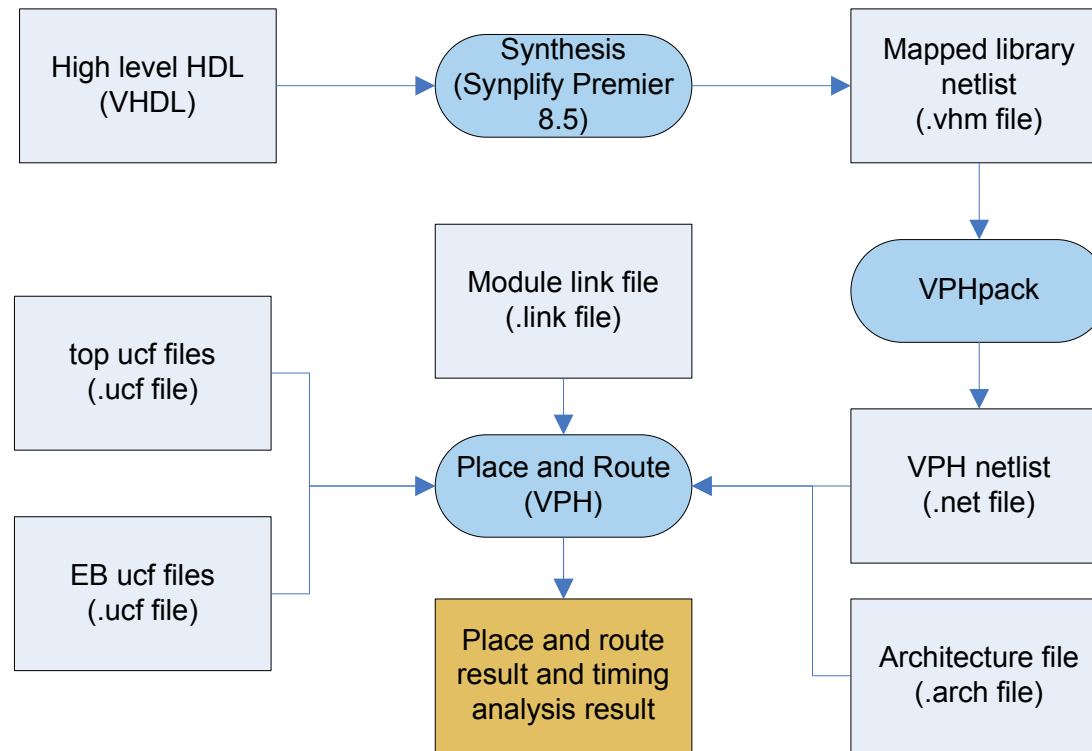


(c) 4x45 CLBs



(d) 2x91 CLBs

6. Exploration Tool – VPH : Versatile Place and Route for Hybrid FPGAs



Design flow of VPH

7. Benchmarks

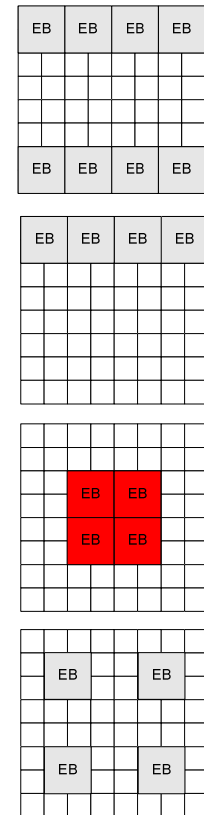
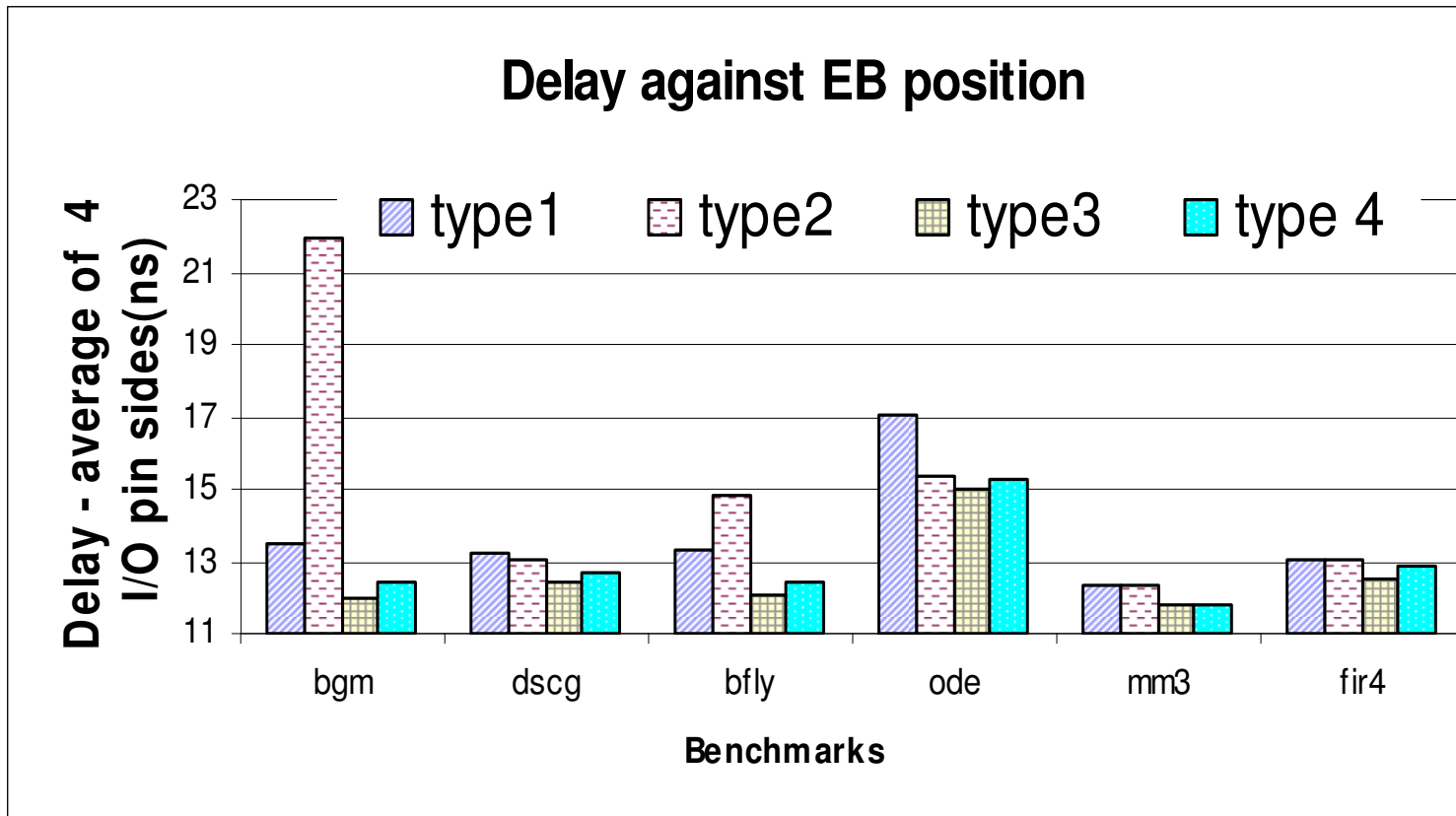
- bgm – Monte Carlo simulations of interest rate model derivatives
- dscg – digital sine cosine generator
- bfly – basic component of Fast Fourier Transform
- ode – ordinary differential equation
- mm3 – 3x3 matrix multiplication circuit
- fir4 – 4-tap finite impulse response filter

Benchmarks	bgm	dscg	bfly	ode	mm3	fir4
No. of CLBs	6433	647	790	336	773	180
No. of FPUs	7	8	8	8	8	8

Number of FPU and CLB used in each benchmarks

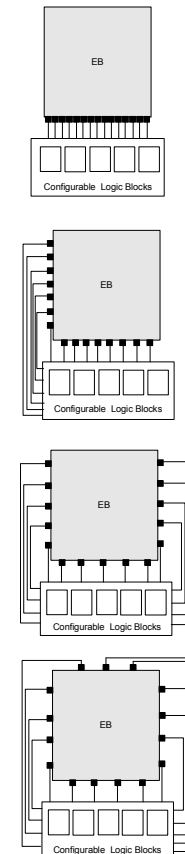
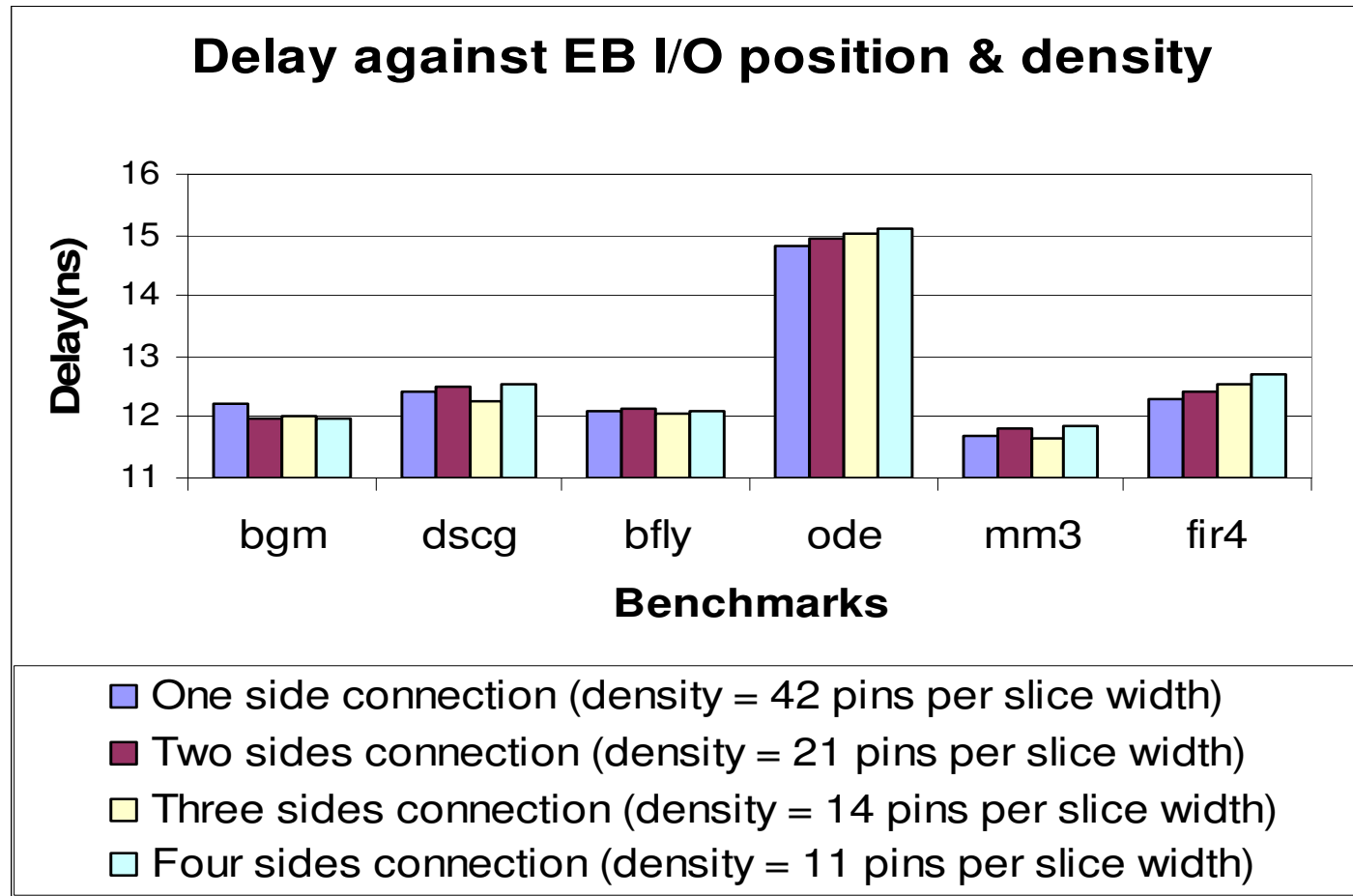
8. Result – 1

EB Position



Result -2

Pin Location – Delay

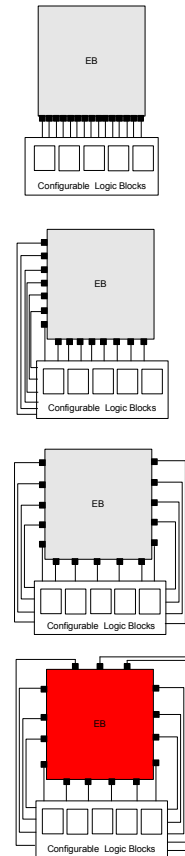


Result -2

Pin Location – Channel width

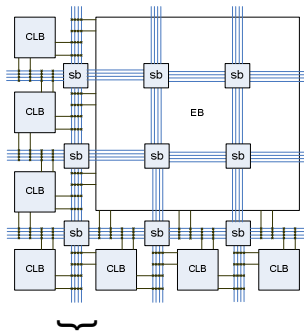
I/O pos.	1 side	2 sides	3 sides	4 sides
Circuit	Min. channel width (Dev. From 1side)			
bgm	46(0%)	35(-22%)	32(-29%)	25(-44%)
dscg	43(0%)	33(-23%)	32(-26%)	32(-26%)
bfly	44(0%)	35(-20%)	33(-25%)	32(-27%)
ode	406(0%)	38(-17%)	37(-20%)	38(-17%)
mm3	42(0%)	40(-5%)	26(-38%)	24(-43%)
fir4	43(0%)	33(-23%)	32(-26%)	30(-30%)

Minimum channel width for different I/O configurations

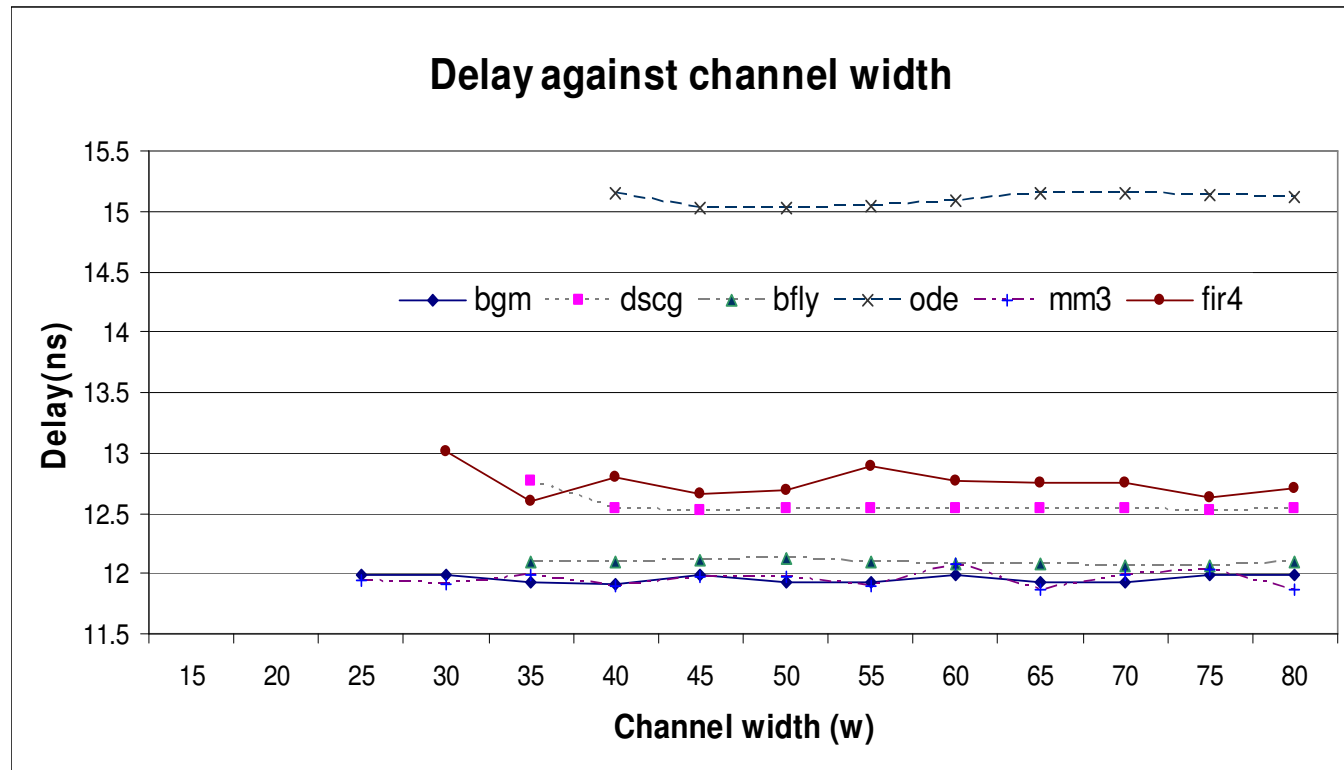


Result-3

Interconnect Flexibility

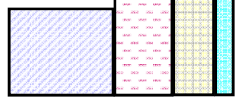


Channel width = w

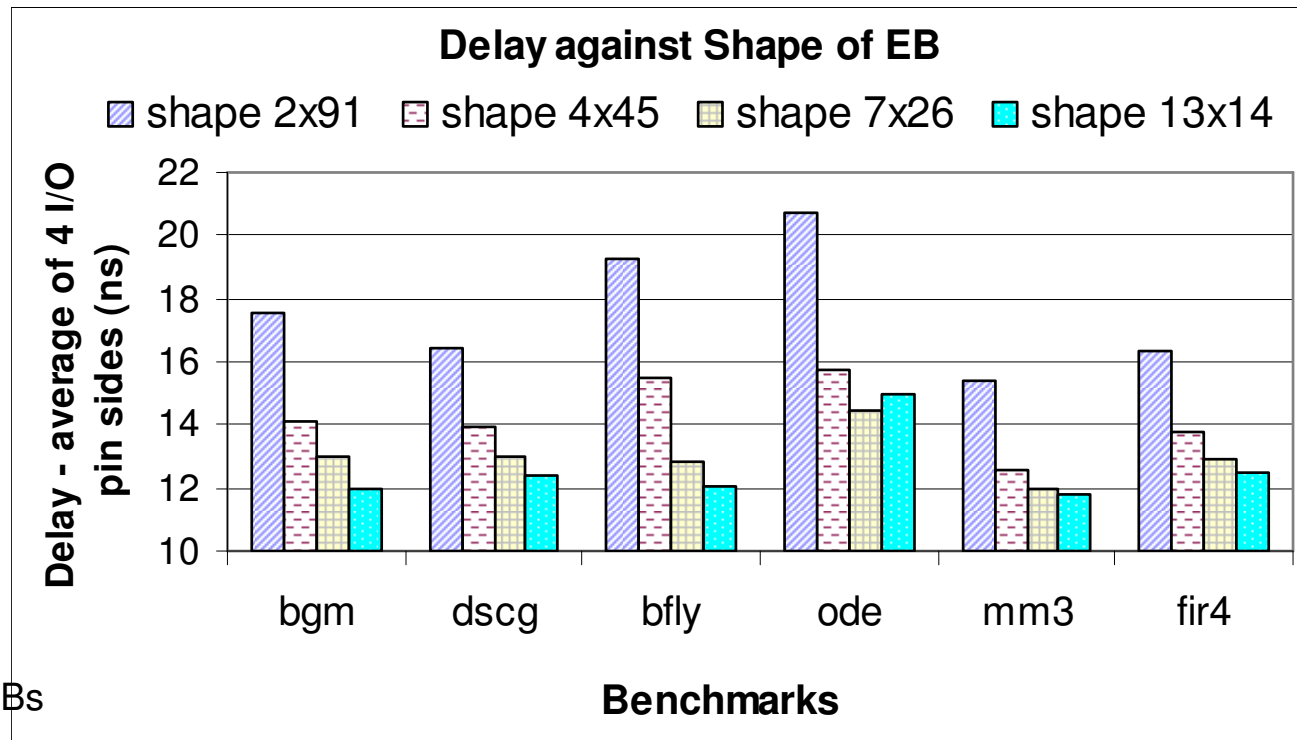


Result-4

Shape



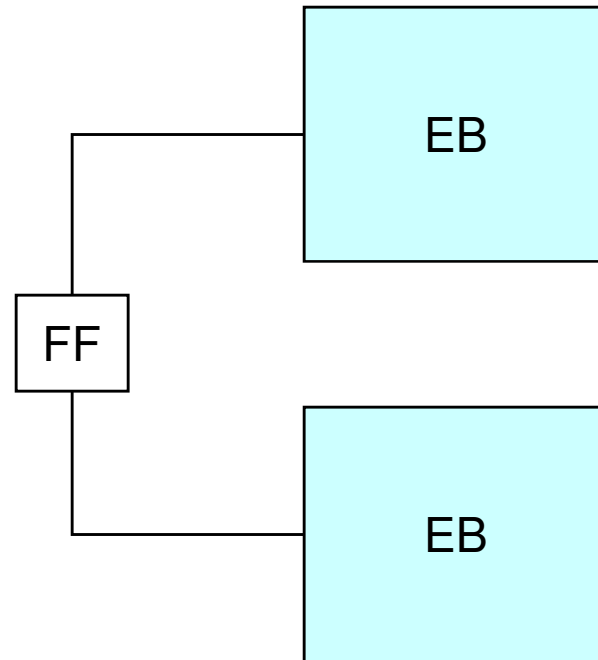
Area \approx 182 CLBs



Result - Discussion

Critical path

-- Routed efficiently once the circuit is routable



9. Conclusion

- Study interconnect between coarse-grained floating point blocks and the fine-grained fabric
- Best interface parameters:
 - EBs close to each other in the middle of the chip
 - Pins distributed evenly around the EB
 - Width of the channels have little impact
 - Square EB is most efficient
- Future: apply approach to FPGAs with other types of embedded blocks