Domain-Specific Hybrid FPGA: Architecture and Floating Point Applications

Chun Hok Ho\textsuperscript{1}, Chi Wai Yu\textsuperscript{1}, Philip Leong\textsuperscript{2}, Wayne Luk\textsuperscript{1}, Steve Wilton\textsuperscript{3}

\textsuperscript{1} Department of Computing, Imperial College London
\textsuperscript{2} Department of Computer Science and Engineering, Chinese University of Hong Kong
\textsuperscript{3} Department of Electrical and Computer Engineering, University of British Columbia

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Overview

1. Motivation
2. Contributions
3. Hybrid FPGA: Architecture
4. Example: Floating-Point FPGA
5. Evaluation
6. Conclusion
1. Motivation

- Heterogeneous blocks in existing FPGAs
  - DSP blocks: DSP48 in Virtex-4
  - Memory blocks: M4K in Cyclone II
- Domain-specific heterogeneous blocks?
  - Identify suitable blocks
  - Architecture exploration
  - Evaluate performance
2. Contributions

- Domain-specific hybrid FPGA architecture
  - Reconfigurable resources: multiple granularity
  - Customised for different applications
  - Modelling: without having to make a chip and write all the CAD tools

- Hybrid FPGA for Floating-Point Applications
  - Novel parameterised coarse-grained block for floating point
  - 6 Benchmarks: compare with Virtex-II device
3. Hybrid FPGA: architecture

- Most digital circuits
  - Datapath ➔ regular, word-based logic
  - Control logic ➔ irregular, bit-based logic

- Hybrid FPGA
  - Coarse-grained resources ➔ datapath
    - Customised coarse-grained block for domain-specific requirements
  - Fine-grained resources ➔ control logic
    - Use existing FPGA architecture
  - Better match to computing applications, particularly in a given domain
Analysis

- Modelling
  - Synthesizable coarse-grained fabric model
  - Use commercial FPGA place and route tool and virtual embedded blocks (VEBs)

- Evaluation
  - P&R different benchmark circuits on hybrid FPGA, measure speed & area

- Exploration
  - Measure performance of benchmarks over different architectures
Virtual Embedded Blocks

• Dummy blocks used to model coarse-grained block’s area and delay

• Timing analyzer can be used to determine hybrid’s performance (including fine-to-coarse routing and delays)
4. Floating point hybrid FPGA

- Coarse-grained units
  - Dominated by multiplication and addition
  - IEEE double precision floating point
  - 64-bit datapaths much more efficient (share routing and configuration, specialised logic)

- Fine-grained units
  - Implement control logic, state machine
  - Xilinx Virtex II used
Coarse-grained fabric design

- Coarse-grained block synthesized
  - HDL to standard cells
  - VEB to model coarse-grained block in Virtex II
- HDL allows parameterisation of architecture
  - Number of embedded floating point operators, feedback registers, etc
Coarse-grained fabric

D=9, M=4, R=3, F=3, 2 add, 2 mul: best density over benchmarks
5. Evaluation

- 6 benchmark circuits
  - DSP computation kernels: e.g. bfly
  - Linear algebra: e.g. matrix multiplication
  - Complete application: e.g. bgm

- Circuits: partitioned to control + datapath
  - Control: vendor tools to fine-grained units
  - Datapath: manually map to coarse-grained units

- Also directly synthesized to Xilinx Virtex II devices for comparison
Example floorplan (bgm)
## Results

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<th>Floating Point hybrid FPGA</th>
<th>XC2V3000-6</th>
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Geo Mean

18.3  2.48
Future work

- Explore different coarse-grained units for floating point
- Automated design tools
- Other domain-specific applications
  - Scientific computing, imaging, networking
6. Conclusion

- Proposed domain-specific hybrid FPGAs
  - Explore architectures using existing FPGA tools
  - Allow customisation beyond conventional FPGAs
- Domain-specific floating point FPGA
  - 18 times area reduction
  - 2.5 times speedup
- Hybrid FPGAs
  - Fine-grained + synthesizable coarse-grained blocks
  - Closer to the area and speed of ASICs
  - Maintain a good degree of flexibility

\{ compared with Virtex-II \}