A TOOL FOR EXPLORING HYBRID FPGAS

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Challenges of hybrid FPGA

- which coarse-grained elements?
- proportion of fine-grained and coarse-grained units?
- interconnection method?
- perform better than existing devices?

Motivation and Contributions

Motivation

- develop an exploration tool to explore hybrid FPGA

Contributions

- adapting VPR to support hybrid FPGA architectures such as the Xilinx Virtex II
- calibrating VPH with existing commercial tools to ensure consistent results
- supporting coarse-grained block modelling via the Virtual Embedded Block (VEB) method
- enabling performance evaluation of domain-specific hybrid with different architectural

Conclusion

- VPH for exploring novel hybrid FPGA
- results are within 20% deviation from commercial tool
- consistent and monotonic to commercial tool
- accurate and flexible performance evaluation of FPGA

VPH – VPR for Hybrid FPGA Architectures

- based on Versatile Placement and Routing(VPR)
- support VEB
- support fast carry chain
- user constraint for position and area
- with embedded memory and multiplier

Design flow of VPH