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Power Characterisation for the Fabric in Fine-Grain Reconfigurable Architectures

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Overview

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6. Implementation and Reporting
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Motivation

- Design challenges for mobile devices
  - Time to market, NRE
  - Logistics
  - Fast evolving standards
- FPGA for mobile applications
  - good: flexible, performance
  - bad: area, power
- Power benchmark
  - Groundhog 2009

Groundhog 2009

- B.0 – Fabric Analysis:
  - Application independent
  - Characterise power consumption of reconfigurable devices in different modes of activity
  - Evaluate low-power modes
  - Evaluate suitability of devices for low-power designs
  - Drive architectural improvements for power efficiency in future devices
- B.1 – B.6
  - Application specific benchmarks (see FCCM09)

Benchmarking Challenges

- Challenges
  - target wide range on devices
  - fair comparison without optimisation potential
  - extensible for future features or architectures
- Previous work
  - often based on MCNC benchmarks
  - circuits small and not representative
  - no stimuli
  - does not target low-power modes

B.0 Fabric Analysis - Basic Concepts

- Use dense and scalable circuit with high toggle rate and without optimisation potential
  - random number generator (RNG)
- Define and characterise power in different processing scenarios
  - “activity modes”
  - includes sleep states
- Characterise thermal aspects of device, how does it heat up during processing

Benchmark Circuit

- Use Random Number Generators (RNG)
  - high logic and routing utilisation
  - high and uniform toggle rate
  - no potential for logic optimisation or optimised placement and routing
  - 512 LUTs/FFs per core
  - scalable, use multiple cores and aim for 90% logic utilisation

Activity Modes

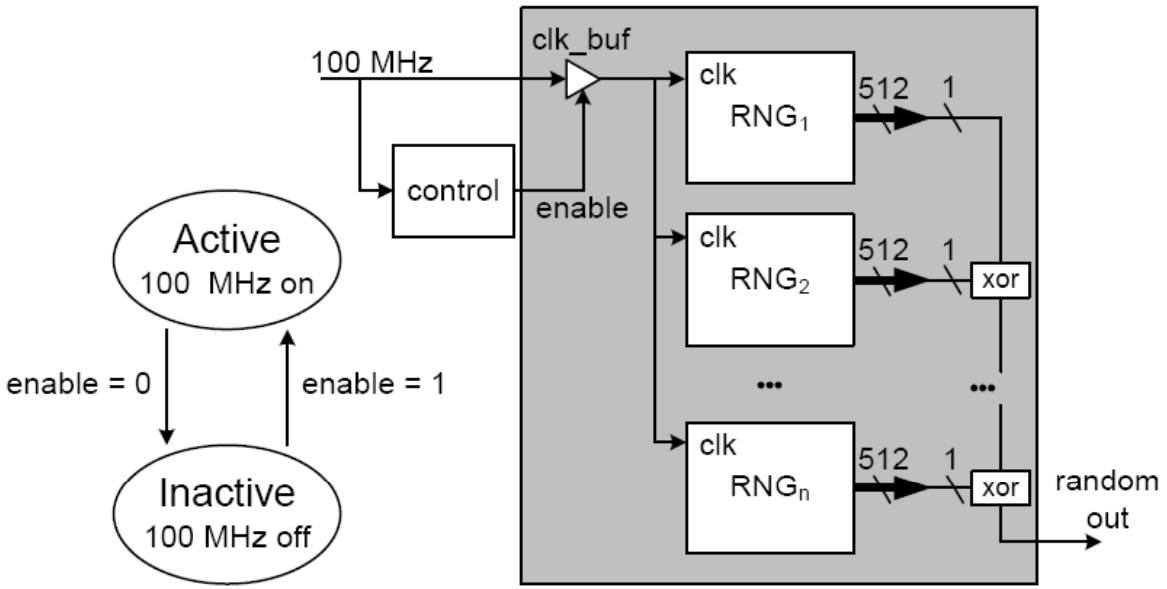
- Measure power in different activation levels rather than looking at dynamic and static power directly
- Activation levels are specified by behaviour
  - active
  - inactive
  - device specific low-power extensions

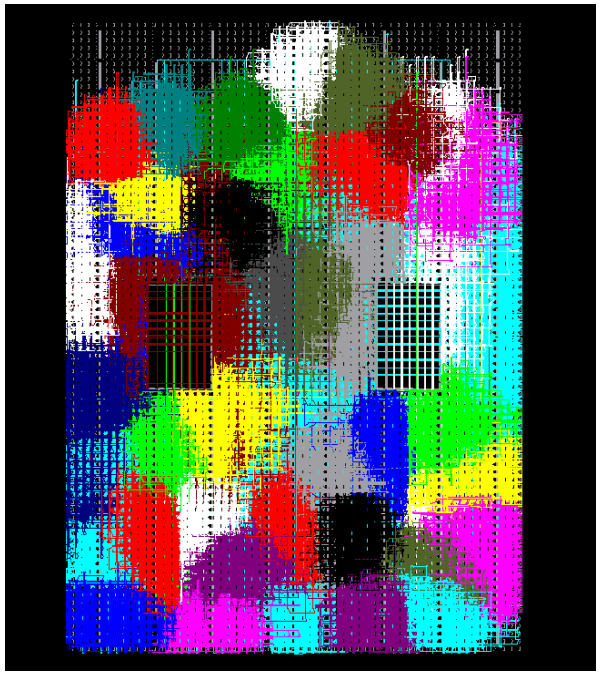
Activity Modes

- Define behaviour of activity modes

	Standard		**Device-specific**	
	Active	Inactive	Sleep	Hibernate
Processing	Yes	No	No	No
Retain State	-	Yes	Yes	No
Wakeup Time	-	Instant	500 µs	50 ms

Implementation



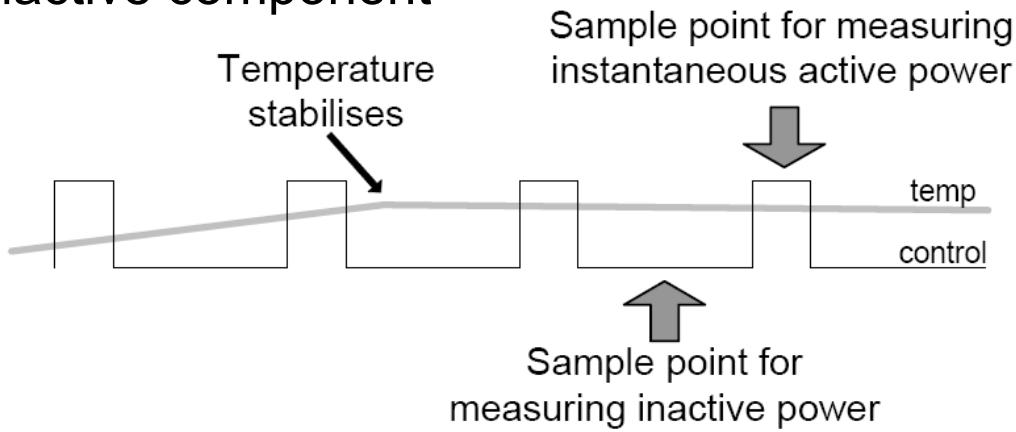


Virtex-II Pro 30
48 RNGs

- Use clock buffer to implement basic activity modes
- External controller switches between “active” an “inactive”
- Connect outputs via XOR chain to avoid logic optimisation

Measurements

- For “cold” devices:
  - measure power in each activity modes
- For “hot” devices:
  - measure over duty cycle:
    - switch between active and inactive
    - vary between 0% - 100%
    - wait until temperature has reached final value
    - measure active and inactive component



Environment and reporting

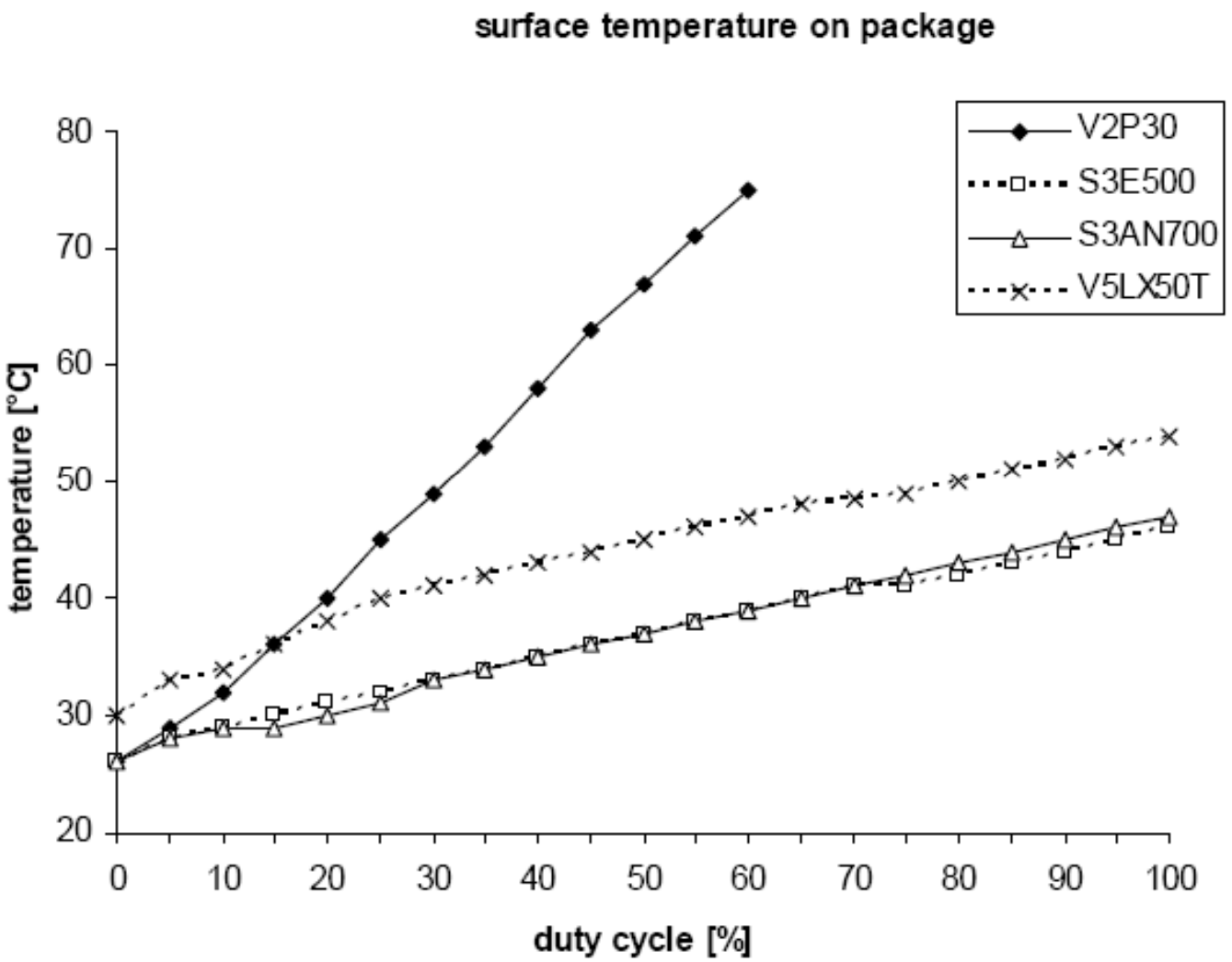
- Reduce environmental influences
  - device on PCB
  - no active cooling, limit airflow
  - ambient temperature 25 °C
- Reporting
  - normalise results to device size
  - diagram and table
  - report all relevant details

Experiment

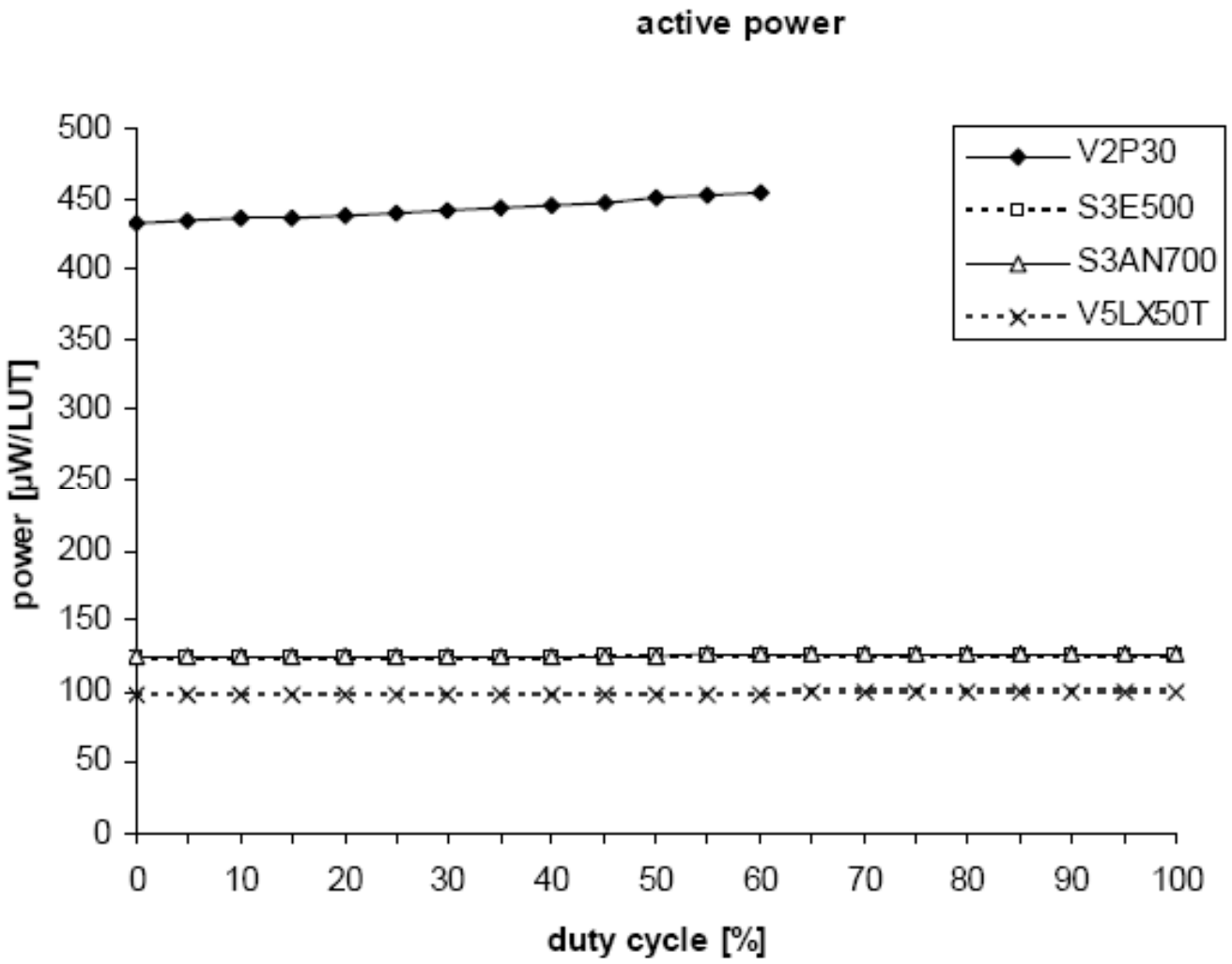
- Fabric analysis of four FPGAs

Device	Process technology	Core voltage	LUTs/FFs
Virtex-II Pro 30	130 nm	1.5 V	27.4 k
Spartan-3E 500	90 nm	1.2 V	9.3 k
Spartan-3AN 700	90 nm	1.2 V	11.8 k
Virtex-5 LX50T	65 nm	1.0 V	28.9 k

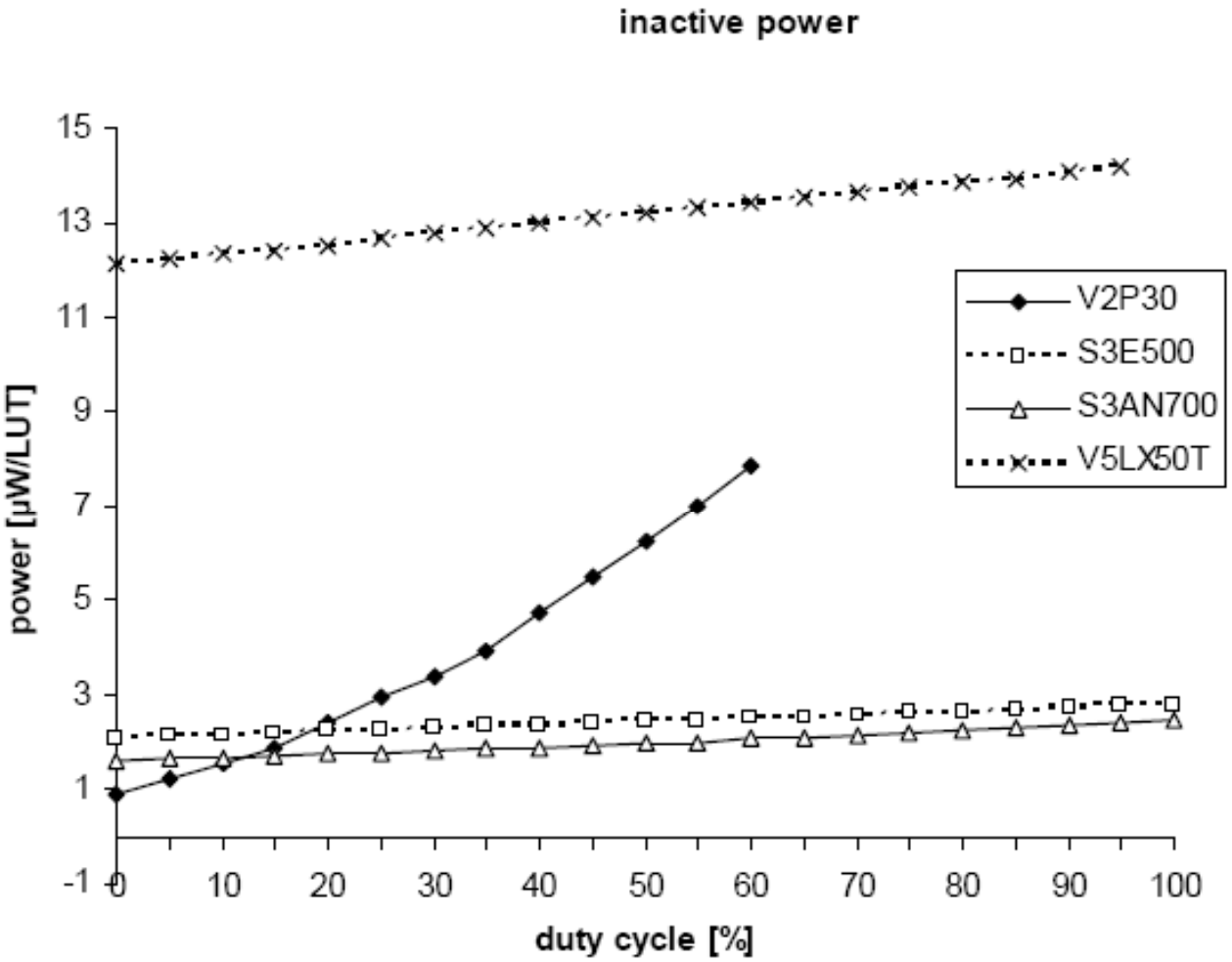
Results - Temperature



Results – Active Power



Results – Inactive Power



Results – Low-Power Modes

- Low-power mode in Spartan-3 FPGAs
  - Disables clock circuits
  - Wakeup time 100 – 500 µs
  - 3x reduction in suspend mode
  - Insufficient for mobile applications, need µW range

	Active	Inactive	Suspend
P_{int} [mW]	1349	18.7	18.1
P_{aux} [mW]	44	43.6	5.8
P_{total} [mW]	1393	62.3	23.9

Xilinx Spartan-3AN 700

Conclusion

- Low-power benchmarks for FPGAs
- B.0: Application independent method for fabric characterisation
- Method based on RNGS and activity modes
- Our measurement show:
  - Process technology improves active power
  - Inactive power increases
  - Lower temperatures reduce deterioration of inactive power
  - Low-power modes currently not sufficient enough
- Download Groundhog 2009:

  http://cc.doc.ic.ac.uk/projects/GROUNDHOG/