GH09.B.2.glue - Glue Logic

General Description

This is a simple glue logic design. The design is built around 3 simple state machines that change based on a sniffing a bus for certain messages. When those messages are detected, the state changes, and counters are turned on in fast, slow, and off modes.

Features

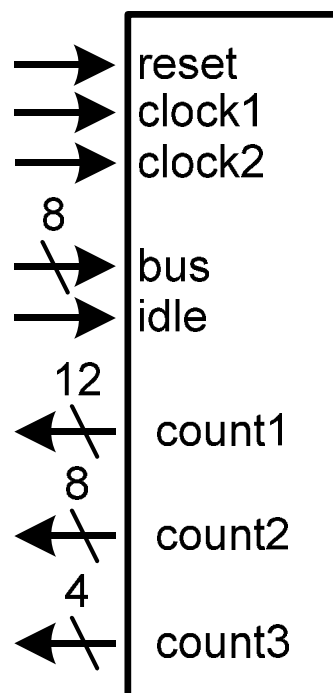- Glue logic with simple state machines and counters.

Block Diagram

*Figure 1 – The chip view of the glue logic*

Details

The basic operation of this design is 3 counters of size 12bits, 8bits, and 4bits endlessly count. These counters can be active with the fast clock (*clock1*), the slow clock (*clock2*), or stopped. These three states (plus one additional state for idle) are controlled by sniffing an 8 bit bus and an idle signal.

Chip Description

Figure 2 shows the state machine design that is replicated three times for each of the counters. The details of the states and transition signals are described below.
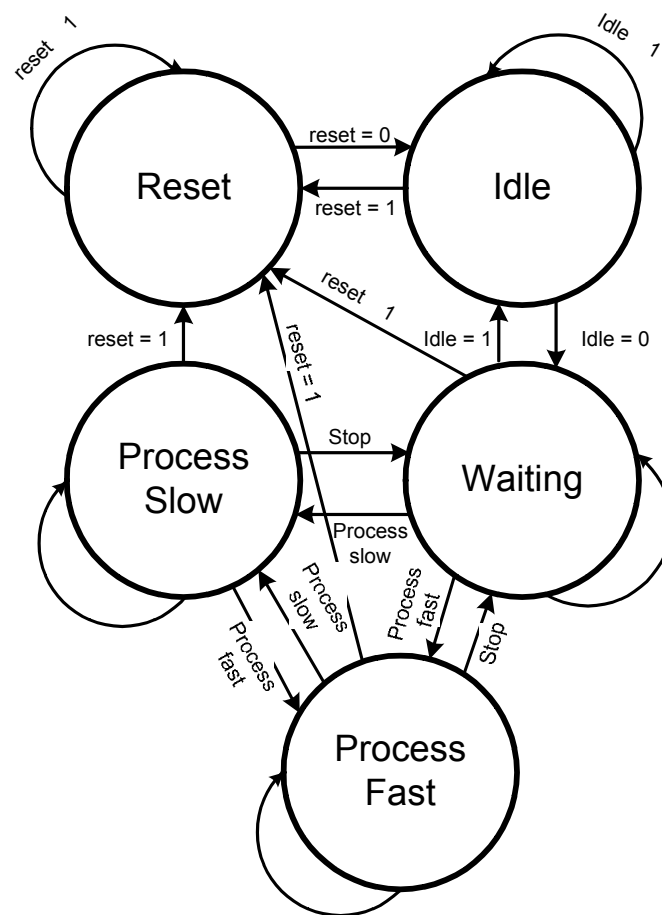
Figure 2 – The state machine design that controls the counters.

In the state Idle the particular state machine is not sniffing the bus. Note that there are only transitions from state Waiting to Idle meaning that if a counter is in a fast or slow counting

state it will not go into the Idle state until a packet is detected that moves the counter into the Waiting state.

In the Process Slow, Process Fast, and Waiting states the bus is continually sampled at the slow clock rate (*clock2*). These three states control the associated counter.

- Process Slow = the counter is counting using the *clock2* input (slow clock).

- Process Fast = the counter is counting using the *clock1* input (fast clock).

- Waiting = the counter maintains its current value.

The transitions between these three states are made depending on the signals on the 8 bit *bus* and the respective counter the state machine is associated with. The transition signals are defined as:

- State Machine 1 controlling Counter 1 (12 bit counter)

    o "00000001" – this is a stop signal and means to go to Waiting.

    o "00000010" – this is the process fast signal to go to Process Fast.

    o "00000011" – this is the process slow signal to go to Process Slow.

- State Machine 2 controlling Counter 2 (8 bit counter)

    o "00000101" – this is a stop signal and means to go to Waiting.

    o "00000110" – this is the process fast signal to go to Process Fast.

    o "00000111" – this is the process slow signal to go to Process Slow.

- State Machine 3 controlling Counter 3 (4 bit counter)

    o "00001101" – this is a stop signal and means to go to Waiting.

    o "00001110" – this is the process fast signal to go to Process Fast.

    o "00001111" – this is the process slow signal to go to Process Slow.

The only other signals that affect the state machine are the *idle* and *reset* signals that are described in the state machine diagram in Figure 2. These signals are universal for each of the three state machines, and therefore, if a reset signal is sent all three state machines would move into the reset state.

The 3 counters (12 bit counter, 8 bit counter, and 4 bit counter) are all the same with the exception that they have different bit widths. Each counter is registered before being output,

and the registering clock signal depends on whether the associated state machine is in process fast or process slow state. These counters are set to zero in the Reset state. In the Wait and Idle state, the value of the counters is maintained. In the Process Fast or Process Slow states the counters increment by +1 for every clock tick from the respective *clock1* (fast clock) or *clock2* (slow clock). Finally, each of the counters will wrap. For example, the 4 bit counter with the current value "1111" binary (F in hexadecimal) is incremented by +1 will have a value of "0000" binary (0 in hexadecimal).