GH09.B.5.bridge - Bridge Conversion

This specifies details about the workloads associated with the GH09.B.5 design.

Input Workloads

The workloads for this benchmark that when combined with this design specification, form a benchmark. The workloads for this design are defined by the following events. Please see the groundhog_09_meta_document.pdf for a description of workloads.

For this design the key input events are:

- reset – the reset signal [signal event]

    o <value0> tag is the associated Boolean value of the signal. Note that the value can be flipped if the designers wish, and the goal is to indicate the initialization of the system.

- write – is a parallel write request on the parallel bus [macro event]

    o <value0> is an integer for the address value on the bus

    o <value1> is the integer of the value to be written

- read – is a parallel read request on the parallel bus [macro event]

    o <value0> is an integer for the address value on the bus

Outputs from the golden functional model tool

The associated output resources that will be generated by the golden functional model are:

- spi_SO - this represents the sequential bit strings from the device to the slave device. This is a macro event that is the serial transfer of the bits [macro event]

    o <value0> is 8 or 24 bits depending on if it is a read or write to the slave. The bits are written in the order of least significant bit (right) to most significant bit. This means that the least significant bit is the R/W bit, the 2nd lsb is the A0 bit in the SPI protocol. See the design spec to help understand these definitions.

- DAT_O – this is the parallel bits on the wishbone compliant bus. [macro event]

    o <value0> is an integer value of the data coming out.